CLAIMS

What is claimed is:

1. A liquid crystal display panel, comprising:

an upper substrate;

a lower substrate parallel to said upper substrate;

a liquid crystal layer between said upper substrate and said lower substrate;

a common line layer having a plurality of common lines on said lower substrate;

a gate line layer having a plurality of gate lines parallel to said common lines on said lower substrate;

an insulating layer on said lower substrate and said common line layer and said gate line layer;

a data line layer having a plurality of data lines perpendicular to said gate lines on said insulating layer;

a plurality of thin film transistors on said lower substrate, where each of said thin film transistors is positioned near a respective intersection portion of said gate lines and said data lines;

a passivation layer on said plurality of thin film transistors and said insulating layer;

a planar insulating layer on said passivation layer;

a plurality of transparent inter-digital pixel electrodes on said planar insulating layer, each of said plurality of transparent inter-digital pixel electrodes having first fingers that extend in the direction parallel to said data lines and are electrically connected to one corresponding drain of said thin film transistors through at least one first contact hole; and

a plurality of transparent inter-digital counter electrodes on said planar insulating layer, one side of each of said plurality of transparent inter-digital pixel electrodes having second fingers that extend in the

direction parallel to said data lines and are electrically connected to one corresponding common line through at least one second contact hole;

wherein a pixel region is defined by one of said data lines and one of said gate lines, at least one said first contact hole and at least one said second contact hole are on the same side of said pixel region, and said first fingers and said second fingers are interlaced in said pixel region.

2. The liquid crystal display panel in claim 1, wherein said plurality of transparent inter-digital pixel electrodes is ITO, IZO, or the combination thereof.

3. The liquid crystal display panel in claim 2, wherein said first fingers are zigzag.

4. The liquid crystal display panel in claim 2, wherein said first fingers are linear.

5. The liquid crystal display panel in claim 1, wherein said plurality of transparent inter-digital counter electrodes is ITO, IZO, or the combination thereof.

6. The liquid crystal display panel in claim 5, wherein said second fingers are zigzag.

7. The liquid crystal display panel in claim 5, wherein said second fingers are linear.

8. The liquid crystal display panel in claim 1, wherein the other side of said transparent inter-digital counter electrodes opposite to said side having said econd fingers is near and parallel to one of said gate lines

in one corresponding pixel region.

9. The liquid crystal display panel in claim 8, wherein said transparent inter-digital counter electrodes overlap said data lines in respective pixel region.

10. A liquid crystal display panel, comprising:

an upper substrate;

a lower substrate parallel to said upper substrate;

a liquid crystal layer between said upper substrate and said lower substrate;

a plurality of common lines and a plurality of gate lines on said substrate and parallel to each other;

an insulating layer on said substrate, said common lines, and said gate lines;

a semiconductor layer on said insulating layer and above said gate lines ;

a plurality of sources and a plurality of drains respectively on two sides of said semiconductor layer above one corresponding gate line;

a plurality of data lines on said insulating layer perpendicular to said plurality of gate lines, and electrically connected to one corresponding source;

a passivation layer on said space, said plurality of sources, said plurality of drains, and said insulating layer;

a plurality of transparent inter-digital pixel electrodes on said passivation layer, each of said plurality of transparent inter-digital pixel electrodes having first fingers that extend in the direction parallel to said data lines and are electrically connected to one corresponding drain through at least one first contact hole; and

a plurality of transparent inter-digital counter electrodes on said passivation layer, one side of each of said plurality of transparent inter-digital pixel electrodes having second fingers that extend in the

direction parallel to said data lines and are electrically connected to one corresponding common line through at least one second contact hole;

wherein a pixel region is defined by one of said data lines and one of said gate lines, at least one first said contact hole and at least one said second contact hole are on the same side of said pixel region, and said first fingers and said second fingers are interlaced in said pixel region.

11. The liquid crystal display panel in claim 10, further comprising a planar insulating layer among said passivation layer, said plurality of transparent inter-digital pixel electrodes, and said plurality of transparent inter-digital counter electrodes.

12. The liquid crystal display panel in claim 11, wherein said plurality of transparent inter-digital pixel electrodes is ITO, IZO, or the combination thereof.

13. The liquid crystal display panel in claim 12, wherein said first fingers are zigzag.

14. The liquid crystal display panel in claim 12, wherein said first fingers are linear.

15. The liquid crystal display panel in claim 11, wherein said plurality of transparent inter-digital counter electrodes is ITO, IZO, or the combination thereof.

16. The liquid crystal display panel in claim 15, wherein said second fingers are zigzag.

17. The liquid crystal display panel in claim 15, wherein said second

fingers are linear.

18. The liquid crystal display panel in claim 10, further comprising a doped amorphous silicon layer having two portions that are between said insulating layer and said plurality of sources, and between said insulating layer and said plurality of drains respectively.

19. The liquid crystal display panel in claim 11, wherein the other side of said transparent inter-digital counter electrodes opposite to said side having said second fingers is near and parallel to one of said gate lines in one corresponding pixel region.

20. The liquid crystal display panel in claim 19, wherein said transparent inter-digital counter electrodes in said pixel region overlap said data lines in respective pixel region.